Please amend the subject application as follows:

IN THE CLAIMS:

Please cancel claims 1-8 and 10 without prejudice, amend claims 9 and 11-16 and add new claims 22 and 23 as follows:

1. - 8. (canceled)

9. (currently amended) A method for manufacturing a capacitor, comprising:

forming a lower electrode in an insulation layer;

forming a dielectric layer on the lower electrode;

forming an upper electrode layer on the dielectric layer;

forming a first protection layer pattern on the upper electrode layer;

etching the upper electrode layer using the first protection layer pattern as an etching mask to form an upper electrode, wherein the first protection layer pattern and the dielectric layer adjacent the upper electrode are partially etched during etching of the upper electrode layer; and

forming a second protection layer enclosing the dielectric layer, the upper electrode and the first protection layer pattern.

10. (canceled)

11. (currently amended) The method of claim [[10]] 9, wherein a thickness of the first protection layer pattern remaining after partial etching is substantially identical to a thickness of the dielectric layer removed by the partial etching.

12. (currently amended) The method of claim [[10]] 9, wherein a thickness of the first protection layer pattern remaining after partial etching is substantially identical to a thickness of the dielectric layer remaining after the partial etching.

13. (currently amended) The method of claim [[10]] 9, wherein a thickness of the second protection layer is substantially identical to a thickness of the dielectric layer removed by partial etching.

14. (currently amended) The method of claim [[10]] 9, wherein a thickness of the second protection layer is substantially identical to a thickness of the dielectric layer remaining after partial etching.

15. (currently amended) A method for manufacturing a semiconductor device, comprising:

forming a first insulation layer on a substrate;

forming a lower wiring and a lower electrode in the first insulation layer;

forming a dielectric layer on the first insulation layer including the lower wiring and the lower electrode;

forming a conductive layer on the dielectric layer;

forming a first protection layer on the conductive layer;

etching the first protection layer to form a first protection layer pattern on the conductive layer;

etching the conductive layer using the first protection layer pattern as an etching mask to form an upper electrode on a portion of the dielectric layer positioned on the lower electrode, wherein the first protection layer pattern and the dielectric layer adjacent the upper electrode are partially etched during etching of the conductive layer;

forming a second protection layer on the dielectric layer and on the first protection layer pattern;

forming a second insulation layer on the second protection layer;

forming a first contact contacting the lower wiring through the second insulation layer;

forming a second contact contacting the upper electrode through the second insulation layer, the second protection layer and the first protection layer pattern; and

forming a first upper wiring on the first contact, and a second upper wiring on the second contact.

16. (currently amended) The method of claim 15, wherein ~~the first protection layer pattern and the dielectric layer adjacent the upper electrode are partially etched during etching of the conductive layer so that~~ the portion of the dielectric layer positioned on the lower electrode protrudes.

17. (original) The method of claim 16, wherein a thickness of the first protection layer pattern remaining after partial etching and a thickness of the second protection layer remaining after the partial etching are substantially identical to a thickness difference between the portion of the dielectric layer positioned on the lower electrode

and a portion of the dielectric layer adjacent the upper electrode.

18. (original) The method of claim 15, wherein the second protection layer is formed on the portion of the dielectric layer positioned on the lower electrode, a sidewall of the upper electrode and a sidewall of the first protection layer pattern.

19. (original) The method of claim 15, wherein the lower electrode comprises one of copper and aluminum, the upper electrode comprises one of titanium nitride and tantalum nitride, and the dielectric layer comprises one of oxide, nitride and a composite of oxide and nitride.

20. (original) The method of claim 15, wherein each of the first protection layer pattern and the second protection layer comprises one of silicon nitride and silicon carbide.

21. (original) The method of claim 15, wherein each of the first upper wiring and the second upper wiring comprises one of copper and aluminum.

22. (new) A method for manufacturing a semiconductor device, comprising:

forming a first insulation layer on a substrate;

forming a lower wiring and a lower electrode in the first insulation layer;

forming a dielectric layer on the first insulation layer including the lower wiring and the lower electrode;

forming a conductive layer on the dielectric layer;

forming a first protection layer on the conductive layer;

etching the first protection layer to form a first protection layer pattern on the conductive layer;

etching the conductive layer using the first protection layer pattern as an etching mask to form an upper electrode on a portion of the dielectric layer positioned on the lower electrode, wherein the first protection layer pattern and the dielectric layer adjacent the upper electrode are partially etched during etching of the conductive layer; and

forming a second protection layer on the dielectric layer and on the first protection layer pattern.

23. (new) A method for manufacturing a semiconductor device, comprising:

forming a first insulation layer on a substrate;

forming a lower wiring and a lower electrode in the first insulation layer;

forming a dielectric layer on the first insulation layer including the lower wiring and the lower electrode;

forming a conductive layer on the dielectric layer;

forming a first protection layer on the conductive layer;

etching the first protection layer to form a first protection layer pattern on the conductive layer;

etching the conductive layer using the first protection layer pattern as an etching mask to form an upper electrode on a portion of the dielectric layer positioned on the

lower electrode;

forming a second protection layer on the dielectric layer and on the first protection layer pattern;

forming a second insulation layer on the second protection layer;

forming a first contact directly contacting the lower wiring through the second insulation layer;

forming a second contact contacting the upper electrode through the second insulation layer, the second protection layer and the first protection layer pattern; and

forming a first upper wiring on the first contact, and a second upper wiring on the second contact.